ABSTRACT

An architecture, circuits, systems and a method for amplifying an analog signal. The architecture and/or circuit generally includes (a) a predriver stage configured to provide an amplified analog output at a first common node, and (b) an adjustable stage comprising independently selectable parallel amplifier segments. The adjustable stage provides an output signal a power range corresponding to the number of selected segments. The output signal has a minimum power efficiency when two or more of the parallel segments are selected. The systems generally include the architecture, circuit or an integrated circuit that embodies one or more of the inventive concepts disclosed herein. The method generally includes the steps of amplifying the analog signal in a fixed amplifier stage, selecting a number of parallel amplifier segments for subsequent signal amplification, and amplifying the amplified analog signal with the activated parallel, selectable amplifier segments to generate an output signal in a unique output power range corresponding to the number of selected parallel amplifier segments. The present invention advantageously provides a relatively compact power amplifier with an extended output power range at which the amplifier is highly efficient. In preferred embodiments, the input and output matching characteristics are generally independent of the number of selected output amplifier segments.